40-Gb/s Analog IC Chipset for Optical Receivers — AGC Amplifier, Full-Wave Rectifier and Decision Circuit — Implemented Using Self-Aligned SiGe HBTs

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***Abstract* — 40-Gb/s analog IC chipset, an AGC amplifier, a full-wave rectifier and a decision circuit, for optical receivers were developed using SiGe HBT technology. The high performance SiGe HBT and optimized circuit configuration make possible an AGC amplifier with a 47.8-GHz bandwidth, a full-wave rectifier, and a decision circuit with 40-Gb/s operation.**

I. Introduction

To realize high-speed and large-capacity communication systems, a transmission system as fast as 40 Gb/s is currently being developed. Several component ICs using various high-speed devices such as Si bipolar transistors [1], HBTs based on SiGe [2][3] and InP/InGaAs [4], GaAs MESFETs [5], and HEMTs [6] have been studied for possible use in a 40-Gb/s system. SiGe HBT is one of the most promising of these devices because it is both inexpensive and highly reliable.

In this paper, we describe 40-Gb/s analog IC chipset, an automatic gain control (AGC) amplifier, a full-wave rectifier, and a decision circuit implemented using SiGe HBT technology for 40-Gb/s optical receivers. The high performance SiGe HBT and optimized circuit configuration, which extracts the device's maximum performance, make 40-Gb/s operation possible.

II. Circuit Configuration

First, we will briefly describe the characteristics of SiGe HBT. The SiGe HBT is fabricated using a 0.2-μm self-aligned selective epitaxial growth process [7]. A boron-doped SiGe-base layer with a thickness of only 15 nm allows a high cut-off frequency of 122 GHz. To reduce parasitic resistance, Ti-salicide layers are formed on poly-Si electrodes. This allows a low base resistance of 90 Ω for an emitter size of 0.2x2 μm. The maximum oscillation frequency is 163 GHz, and the ECL gate delay is 5.5 ps.

A. AGC amplifier

A block diagram of the AGC amplifier is shown in Fig. 1. In the signal path, there is an input buffer (IB), two variable gain amplifier stages (VGA), and an output buffer (OB) with a constant gain. A peak detector (PD) outputs signals (PD0 and PD1) in proportion to the output amplitude of out0 and out1. Another output (PDM) is used as a reference voltage. The PDM voltage is equal to PD0 and PD1 when there is no signal input. According to the outputs of PD, a gain control circuit (GC) controls the gain of the VGAs. To compose an AGC feedback loop, several external amplifiers and a low pass filter are necessary.

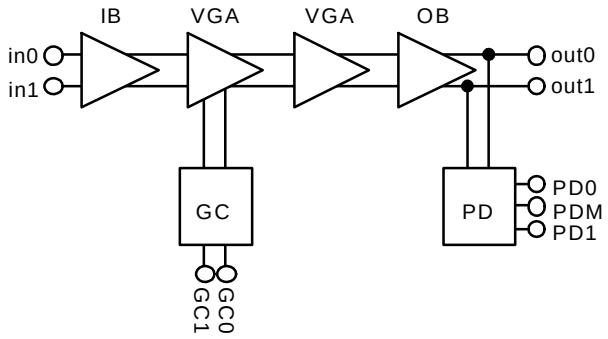


Fig. 1. Block diagram of AGC amplifier.

The two VGAs have the same circuit configuration shown in Fig. 2. Each VGA consists of a Gilbert multiplier. The signals (i0 and i1) are input to the lower transistor pair (Q1, Q2) and the gain control signals (VCNT0 and VCNT1) are input to the upper transistor pair (Q3-Q6) in the gain control stage. It is known that the bandwidth at the gain control stage decreases as the gain of the VGA decreases [3][8].

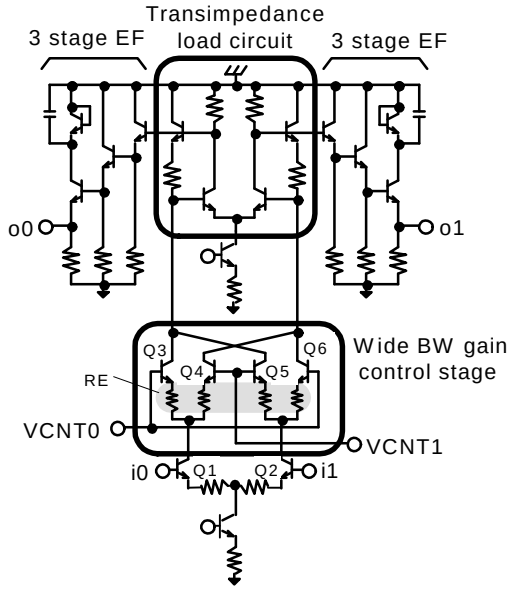


Fig. 2. Schematic of variable gain amplifier (VGA).

We solved this problem by adding bandwidth-compensating resistors to the emitter of Q3-Q6. The current gain of the gain control stage (G_i) is expressed as

$$G_i(s) \approx \frac{G_{i0}}{(1+s\tau_F)(1+s\alpha\tau_F)} \quad (1)$$

$$G_{i0} = \frac{g_{m3} - g_{m4}}{g_{m3} + g_{m4} + 2R_E g_{m3} g_{m4}} \quad (2)$$

$$\alpha = \frac{2(r_b + R_E) g_{m3} g_{m4}}{g_{m3} + g_{m4} + 2R_E g_{m3} g_{m4}} \quad (3)$$

where g_{m3} and g_{m4} are the transconductance, τ_F is the base transit time, and r_b is the base resistance of Q3 and Q4. The bandwidth of G_i is expressed as

$$\omega_{BW} = \frac{1}{\tau_F}\sqrt{\frac{\sqrt{(1+\alpha^2)^2 + 4\alpha^2} - (1+\alpha^2)}{2\alpha^2}} \quad (4)$$

Figure 3 shows the bandwidth dependence on the normalized collector current of Q3 (IC3). The bandwidth (ω_{BW}) has a minimum value when IC3/(IC3+IC4) = 0.5, that is IC3 = IC4 ($g_{m3} = g_{m4}$). This is because α has a maximum value when $g_{m3} = g_{m4}$. As can be seen in the figure, the bandwidth-compensating resistor RE mitigates this tendency. The simulation results show that no bandwidth degradation occurs when RE = 30 Ω.

A peaking technique is also effective in achieving a wide bandwidth, so a transimpedance circuit is used as a load circuit. The transimpedance load circuit has a peaking effect due to its feedback loop. However, peaking should be carefully controlled because excessive peaking degrades the flatness in the frequency response, resulting in waveform distortion [3].

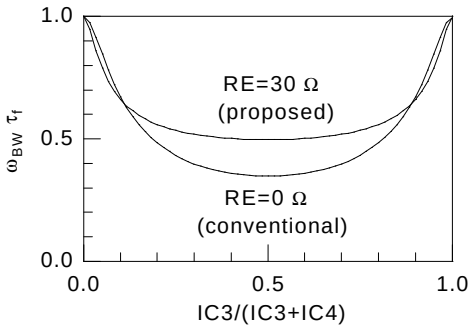


Fig. 3. Bandwidth dependence on the operating current (IC3) in the gain control circuit.

B. Full-wave rectifier

Figure 4 shows the block diagram of the full-wave rectifier. The full-wave rectifier is composed of an input buffer (IB), a full-wave rectifier (FR), an amplifier (AMP), and an output buffer (OB). The input signal is rectified by FR, and is amplified by AMP and OB, both of which have a gain of 10 dB. The schematic of the FR is shown in Fig. 5. A transimpedance load circuit is used in FR to improve the bandwidth. The rectifier is composed of a wired-OR circuit of differential signals. The transimpedance load circuit and triple stage EF are also used in the AMP and OB.

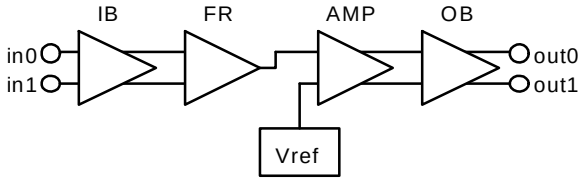


Fig. 4. Block diagram of full-wave rectifier.

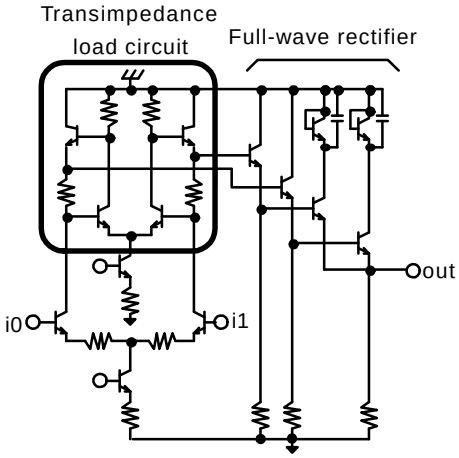


Fig. 5. Schematic of full-wave rectifier (FR).

C. Decision circuit

Figure 6 shows the block diagram of the decision circuit. The decision circuit is composed of an input buffer (IB), a two-stage preamplifier (Pre1, 2), a master-slave flip-flop (MS-FF), a pre-output buffer (PB), an output buffer (OB), and a clock buffer (CB). The triple stage EFs are used as the input and clock buffers. The total gain of the two-stage preamplifier is 22 dB. The schematic of the preamplifier is shown in Fig. 7. A transimpedance load circuit is used in Pre1 to widen the bandwidth, and a cascode amplifier is used in Pre2 because the output level of Pre1 is too low to drive the MS-FF.

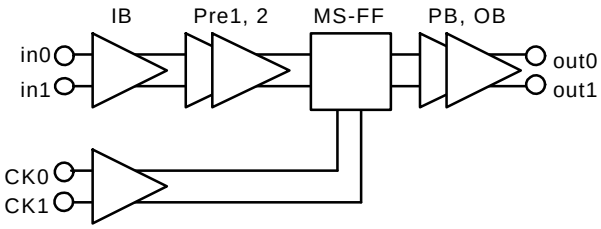


Fig. 6. Block diagram of decision circuit.

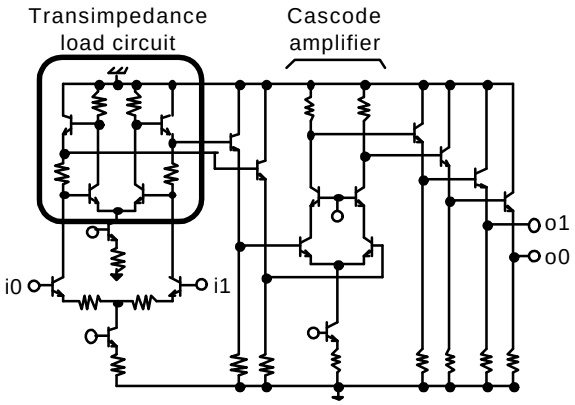


Fig. 7. Schematic of two-stage preamplifier in the decision circuit.

III. Experimental Results

The gain versus frequency characteristics of the AGC amplifier measured using an on-wafer RF probe are shown in Fig. 8. A bandwidth of 47.8 GHz was achieved at a maximum gain of 21.5 dB, and the bandwidth was 48.3 GHz at a minimum gain of 0.5 dB. The small fluctuation in the bandwidth when the gain was changed can be attributed to the bandwidth-compensating resistor in the VGA.

The AGC amplifier module and its frequency response are shown in Fig. 9. The AGC amplifier chip was mounted to an alumina substrate using ribbon bonding. RF signals were propagated through V-connectors and co-planar transmission lines on the alumina substrate, and the signal loss at 40 GHz was about 4 dB. A flat frequency response was obtained up to 35 GHz (Fig. 9 (b)). Figure 10 shows the operational waveform of the AGC amplifier module. A 40-Gb/s pseudorandom bit stream was generated using 10-Gb/s PPG and a 4:1 multiplexer module [9]. A well-opened eye pattern was obtained at 40 Gb/s.

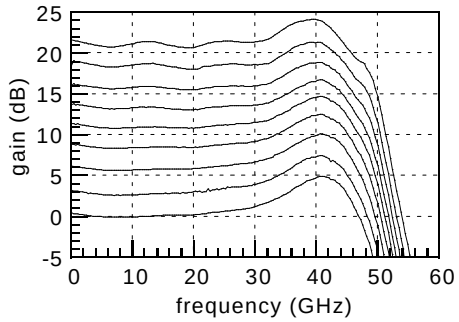
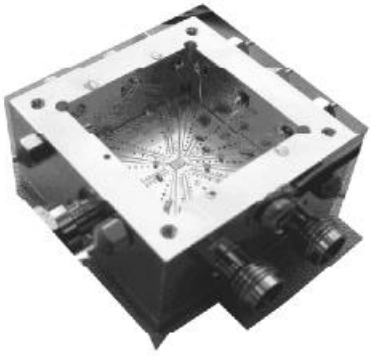
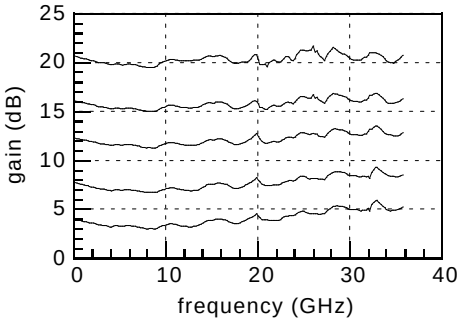


Fig. 8. Gain versus frequency characteristics of AGC amplifier (on-wafer).



(a)



(b)

Fig. 9. (a) AGC amplifire module, (b) gain versus frequency characteristics of AGC amplifier module.

The operational waveform of the full-wave rectifier was measured using an on-wafer RF probe as shown in Fig. 11. A clear output waveform was obtained at 40 Gb/s, and a 90-mVpp 40-GHz clock signal was obtained through a

bandpass filter. Figure 12 shows the operational waveforms of the decision circuit measured using an on-wafer RF probe. A well-opened eye pattern was obtained at 40 Gb/s.

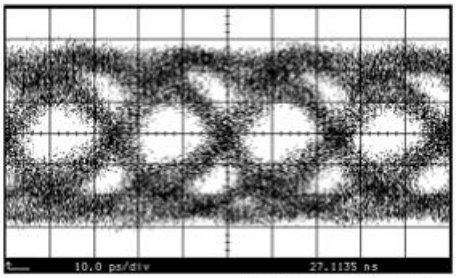


Fig. 10. Operational waveform of AGC amplifier module at 40 Gb/s.

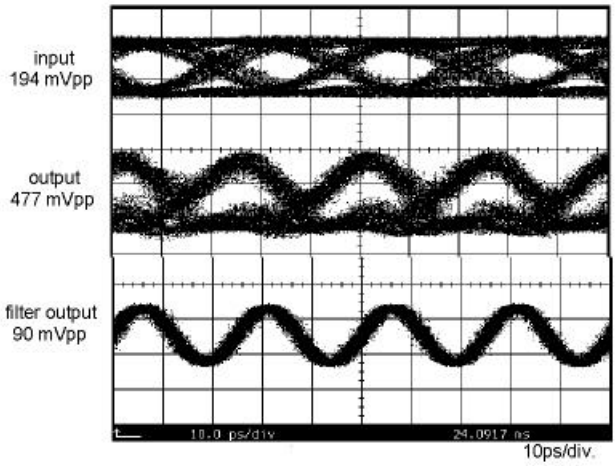


Fig. 11. Operational waveform of full-wave rectifier at 40 Gb/s (on-wafer).

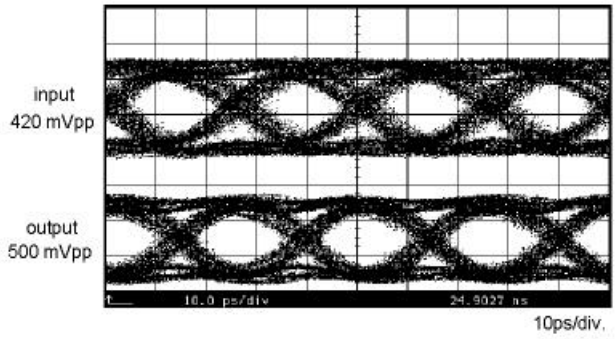


Fig. 12. Operational waveform of decision circuit at 40 Gb/s (on-wafer).

The three kinds of chips were measured to be 1.2x1.8 mm. The supply voltage of the AGC amplifier and the full-wave rectifier was -7.5 V, and their power dissipations were 1.2 and 1.6 W, respectively. The supply voltage of the decision circuit was -5.2 V, and its power dissipation was 0.9 W.

IV. Conclusion

An AGC amplifier, a full-wave rectifier, and a decision circuit for 40-Gb/s optical receivers were developed using SiGe HBT technology. The high performance SiGe HBT and optimized circuit configuration make possible an AGC amplifier with a 47.8-GHz bandwidth, a full-wave rectifier, and a decision circuit with 40-Gb/s operation.

We have already reported on a preamplifier with a 45-GHz bandwidth, a limiting amplifier with a 49-GHz bandwidth, and a 40-Gb/s 1:4 DEMUX implemented in SiGe HBT technology [2]. A 40-Gb/s optical receiver can be composed using these ICs, thus proving the effectiveness of SiGe HBT technology for 40-Gb/s optical systems.

Acknowledgement

The authors would like to thank Dr. Y. Kiyota, E. Ohue, K. Oda, R. Hayami, M. Tanabe, H. Shimamoto, Dr. M. Kondo, K. Ishikawa, K. Watanabe, and R. Takeyari for their valuable discussions.

References

[1] A. Felder, et al., "30 GHz Static 2:1 Frequency Divider and 46 Gb/s Multiplexer/Demultiplexer ICs in a 0.6 µm Si Bipolar Technology," in Dig. Tech. Symp. on VLSI Circuits, 1995, pp. 117-118.

[2] T. Masuda, et al., "45 GHz Transimpedance 32 dB Limiting Amplifier and 1:4 High-Sensitivity Demultiplexer with Decision Circuit using SiGe HBTs for 40 Gb/s Optical Receiver," in Dig. Tech. IEEE ISSCC, 2000, pp. 60-61.

[3] K. Ohhata, et al., "Design Aspects of 32.7-GHz Bandwidth AGC Amplifier IC with Wide Dynamic-Range Implemented in SiGe HBT," in Proc. BCTM, 1998, pp. 39-42.

[4] H. Suzuki, et al., "InP/InGaAs HBT IC's for 40 Gbit/s optical transmission systems," in Tech. Dig. IEEE GaAs IC Symp., 1997, pp. 215-218.

[5] K. Sano, et al., "44 Gbit/s GaAs MESFET selector IC," in Electron. Lett., July 1997, vol. 33, no. 16, pp. 1377-1379.

[6] T. Otsuji, et al., "An 80-Gbit/s Multiplexer IC Using InAlAs/InGaAs/InP HEMT's," in IEEE J. Solid-State Circuits, vol. 33, no. 9, pp. 1321-1327, Sept. 1998.

[7] K. Washio, et al., "82 GHz Dynamic Frequency Divider in 5.5 ps ECL SiGe HBTs," in Dig. Tech. IEEE Int. Solid-State Circuits Conf., 2000, pp. 210-211.

[8] M. Möller, et al., "13 Gb/s Si-Bipolar AGC Amplifier IC with High Gain and Wide Dynamic Range for Optical-Fiber Receivers," in IEEE J. Solid-State Circuits, vol. 29, no. 7, pp. 815-822, July 1994.

[9] T. Masuda, et al., "40 Gb/s, 4:1 Multiplexer and 1:4 Demultiplexer IC Modules using SiGe HBTs," in Dig. Tech. IEEE IMS 2001, TH2F-2.